

**Cambridge Microprocessor  
Systems Limited  
307-Module  
Hardware**

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### **Important**

The sections of code contained in this manual are not necessarily written to operate with any software supplied with the board. many of them are written so that they can be blown directly into EPROM once they have been assembled. Other code segments may not be programs at all but just examples to demonstrate a particular point.

Throughout this manual the K-307M board is referred to as the 307-Module. Other options of the board include K-307G (Graphics LCD compatible) and K-0307V (Vacuum fluorescent display compatible).

## **1 Introduction**

The 307-Module is a small single board computer which combines a high performance 32/16/8 bit processor with a wide range of on board peripherals to provide a unique level of hardware and software performance for the OEM designer and system integrator. The board measures just 100 x 118 mm and is based around the 68307 microcontroller. The 68307 is a powerful 68000 compatible microcontroller manufactured by Motorola. It is one of a family of devices using a 68EC000 core.

The I/O provided on the 307-Module includes a complete 8 bit analogue interface, digital I/O, a keypad interface, LCD display driver and a serial port that can be used for multi drop networks with an RS-485 interface or to connect to a P.C. with an RS-232 interface. Also, provided by the microcontroller, are 16 bit two timer counters.

The 307-Module also includes a full 16 bit 68000 expansion bus allowing a number of peripheral boards to be connected. Compatible peripheral boards include video controllers, fast 12 bit analogue inputs and outputs, up to 8 serial I/O ports and digital I/O including a centronics printer interface. Bus interfaces are also provided to 8051 peripherals and M-bus peripherals. The M-bus port is compatible with the I<sup>2</sup>C bus which is a proprietary Philips interface bus.

Low power modes of operation can be achieved by slowing down the operation of the CPU or putting it to sleep altogether since it is a fully static

core. Power consumption can also be reduced by turning off the clock signals to the on chip peripherals.

When used with a starter pack containing a high level programming language and the Minos operating system, all the features of the 307-Module are very easy to use and development time can be minimal. Minos is a royalty free real time operating system that is designed specifically for embedded applications. It enables very easy connections to and operation of peripheral devices, advanced memory management, full round robin multi tasking and interprocess communication. For full details on the Minos operating system please see the appropriate documentation.

This section of the manual is designed to give users all the information required to configure the 307-Module and add peripherals on the expansion bus. Also included is a description of the CPU and its registers. For full details on the CPU and its registers we recommend you obtain a copy of the CPU user manuals and data sheets, details in the appendix.

## **2 The MC68307 Microcontroller**

The MC68307 is an advanced 32/16/8 bit microcontroller based on the industry standard 68000 microprocessor. The MC68307 integrates the 68000 core with a 68681 type serial port, a timer module, a M-bus module, some digital I/O lines, bus interface logic and up to 9 interrupt lines. The bus interface logic also includes chip select logic, which is used on the 307-Module to generate the chip selects for the RAM, ROM and peripheral and memory address strobes.

### **2.1 The 68000 CPU**

The CPU contained within the MC68307 is a version of the standard 68000 with full software compatibility with other members of the 68000 family. The MC68307 uses the 68EC000 core which has been optimized for use in embedded applications. This version of the 68000 does not support E cycles for 6800 type peripherals. For a full list of the features of this CPU core please see the manufacturers data sheet on the 68EC000, details in the appendix.

The 68EC000 core used on the MC68307 is fully static. This means that the CPU clock can be reduced or even turned off completely to save power while the CPU is not doing much. When the processor is woken up to perform a task it picks up all its registers as they were left when it was stopped. For more details on the low power modes please see section 2.6.

#### **2.1.1 Exception Processing**

The exception processing state is entered when the processor performs interrupt services, trap instructions and tracing. The exception can be generated internally by executing an instruction or externally by generating an interrupt, a reset or a bus error. A table of exception vectors for the MC68307 is shown below. Unassigned or reserved vectors should never be used. All exception vectors are accessed in Supervisor Data (SD) mode except the reset vector which is accessed in Supervisor Program (SP) mode.

Vector Number	Address Decimal	Address Hex	Address Space	Vector Assignment
0	0	000	SP	Reset Initial SSP
1	4	004	SP	Reset Initial PC
2	8	008	SD	Bus Error
3	12	00c	SD	Address Error
4	16	010	SD	Illegal Instruction
5	20	014	SD	Zero Divide
6	24	018	SD	CHK Instruction
7	28	01C	SD	TRAPV Instruction
8	32	020	SD	Privilege Violation
9	36	024	SD	Trace
10	40	028	SD	Line 1010 Emulator
11	44	02C	SD	Line 1111 Emulator
12	48	030	SD	(Unassigned, Reserved)
13	52	034	SD	(Unassigned, Reserved)
14	56	038	SD	(Unassigned, Reserved)
15	60	03C	SD	Uninitialised Interrupt
16 - 23	64 - 92	040-05C	SD	(Unassigned, Reserved)
24	96	060	SD	Spurious Interrupt by BERR
25	100	064	SD	(Unassigned, Reserved)
26	104	068	SD	(Unassigned, Reserved)
27	108	06C	SD	(Unassigned, Reserved)
28	112	070	SD	(Unassigned, Reserved)
29	116	074	SD	(Unassigned, Reserved)
30	120	078	SD	(Unassigned, Reserved)
31	124	07C	SD	(Unassigned, Reserved)
32 - 47	128-188	080-0BC	SD	Trap Instruction Vectors
48 - 59	192-236	0C0-0EC	SD	(Unassigned, Reserved)
60 - 63	240-252	0F0-0FC	SD	System Con fig.. Registers

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Vector Number	Address Decimal	Address Hex	Address Space	Vector Assignment
64 - 255	256-1020	100-3FC	SD	User Interrupt Vectors

### 2.1.2 Interrupt Controller

The interrupt controller on the MC68307 is used to handle all the interrupt sources to the processor. Interrupts can be generated by the on chip peripherals i.e. UART, timers, M-bus etc.; or the external interrupts i.e. INT1 to INT8 and NMI. The interrupt controller will receive the interrupt request from the peripheral, it will then prioritize it before passing the highest priority request valid at any time on to the processor. When the processor responds to the interrupt request with an interrupt acknowledge cycle the interrupt controller will provide the correct vector number for the peripheral generating the interrupt.

There are nine external interrupt sources. The first, and the one with the highest priority, is NMI or IRQ7. This signal always has a priority level of 7 and it will always be dealt with first by the processor. It is not possible to turn this interrupt source off. The other eight interrupt sources are labeled INT1 to INT8. Each of these sources can be programmed to generate any level interrupt or disabled if required. The interrupt controller includes a daisy chain decoder for when there is more than one interrupt pending for a particular level. In this chain NMI has the highest priority, followed by INT1 to INT8, Timer 1, Timer 2, UART and the M-bus with the lowest priority. For a description on how to set up the interrupts please see section 6. On Minos systems INT1 is set to level 1, INT2 to level 2 etc..

On the 307-Module, INT1 is used by the M-bus devices on the keypad port. INT2 is used by the real time clock. This is pulsed at 1 Hz. INT3, INT4, INT7 and INT8 are general purpose back plane interrupts connected to I1, I2, I3 and I4 respectively. INT3 is used by most of the CMS peripheral boards. INT5 is used by digital I/O port 0 and INT6 is used by digital I/O port 1.

### 2.1.3 Interrupt Vector Generation

The interrupt controller passes the highest priority interrupt request to the processor. The processor responds with an IACK signal to receive a vector number. The vector number is used by the processor to access the interrupt service routine. The interrupt controller will provide the vector of the highest priority interrupt source currently pending. The vector is made up of two four bit parts. The most significant part is provided by the Peripheral Interrupt Vector Register (PIVR). This will select a block of memory to use for the vector table. The least significant four bits are encoded by the interrupt controller depending on the source. The table below gives the vector numbers for the different interrupt sources. On Minos systems PIVR = \$40.

Vector	Interrupt Source
PIVR+\$00	Spurious Interrupt
PIVR+\$01	IRQ7 Input
PIVR+\$02	INT1 Input
PIRV+\$03	INT2 Input
PIVR+\$04	INT3 Input
PIVR+\$05	INT4 Input
PIVR+\$06	INT5 Input
PIVR+\$07	INT6 Input
PIVR+\$08	INT7 Input
PIVR+\$09	INT8 Input
PIVR+\$0A	Timer 1
PIVR+\$0B	Timer 2
PIVR+\$0C	UART Module
PICR+\$0D	M-bus Module

To calculate the memory location for the service routine the value contained in the PIVR is added to the interrupt source vector number. In Minos systems this value is set to \$40. The result is then multiplied by four to get a 32 bit address. This address is the start address of the interrupt service routine. As an example, if timer 1 generates an interrupt the vector number will be \$4A.

When this is multiplied by four to get an address we end up with \$128. This address is in the EPROM which can not contain the service code. The data at address \$128 will be a jump table to another address which will be in RAM. This will be the interrupt service routine. The Crossware C Support includes high level language support for handling interrupts from C functions.

#### 2.1.4 Function Codes

The 68000 can operate in two different modes. Each mode can support two different cycle types. The current mode of operation is defined by the state of three signals on the 68000 CPU. These signals are not available externally on the MC68307 but they can be used by the address compare logic for the chip selects. This allows a chip select to be asserted in particular modes of operation only. When the processor is in supervisor mode it has access to all the system resources and all instructions can be executed. Both operating system calls and exception processing is done in supervisor mode. In user mode the processor can not access system configuration registers and some instructions are not allowed. Most programs will run in user mode to prevent them from being able to over write system dependent registers. The table below shows the state of the Function Code signals for each mode of operation.

FC2	FC1	FC0	Cycle Type
0	0	0	Undefined, Reserved
0	0	1	User Data
0	1	0	User Program
0	1	1	Undefined, Reserved
1	0	0	Undefined, Reserved
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	Interrupt Acknowledge

The interrupt acknowledge function code should never be programmed into the chip select registers on the MC68307.

## 2.2 The Bus Interface

This section handles all accesses to devices outside the microcontroller, whether it is a 68000 access or an 8051 bus access. Also contained in this section is the chip select logic and DTACK delay generator. The memory map used by the 307-Module is determined by settings in the chip select registers. The addresses given below are those used when the 307-Module is used with the Minos operating system. There must always be EPROM at address \$000000 to provide a reset vector.

### 2.2.1 Main Memory Map

The main memory map is a 2 M-byte block of memory that the 307-Module uses. This for compatibility with Mini-Module systems. The 307-Module memory map can be enlarged to enable larger EPROMs to be fitted.

	Size	Start Address	End Address
EPROM	512 k-byte	\$000000	\$07FFFF
RAM	512 k-byte	\$080000	\$0FFFFFF
	128 k-byte	\$080000	\$09FFFF
LCD	64 k-byte	\$100000	\$10FFFF
Watchdog	64 k-byte	\$110000	\$11FFFF
Local I/O	4 k-byte	\$120000	\$120FFF
Reserved	28 k-byte	\$121000	\$127FFF
Peripheral I/O	32 k-byte	\$128000	\$12FFFF
Memory Expansion	832 k-byte	\$130000	\$1FFFFFF

### 2.2.2 Local Memory Map

The local memory map contains all the on board peripherals. The base address of these devices is determined by the setting in the Module Base Address Register (MBAR). This block of memory takes up 4 k-bytes.

	Start Address	End Address
Port A	\$120010	\$120015
Port B	\$120016	\$12001B
Interrupts	\$120020	\$120027
UART	\$120100	\$12011F
Timers	\$120120	\$120139
M-bus (I <sup>2</sup> C)	\$120140	\$120149

Other addresses within the range \$120000 to \$120FFF are reserved and should not be used.

### 2.2.3 Chip Selects

The MC68307 can generate four chip selects that can be used to divide up the memory map. The chip selects on the 307-Module are programmed to generate the main memory map given in section 2.2.1. For each chip select there are two registers in the microcontroller. The first will determine the base address of the chip select block and what function code must be present for it to be selected. The second register defines the size of the chip select block and the number of wait states inserted before the end of the cycle. Using these two registers it is possible to allow an area of memory to be accessed for reading or writing only, in supervisor or user modes. All the chip selects on the 307-Module are programmed for 16 bit accesses in any mode of operation, using 68000 bus cycles.

The first chip select, CS0, is used on the 307-Module to decode the EPROM. This select line has no wait states inserted allowing EPROMs as slow as 200 ns to be used.

The second chip select, CS1, is used to decode the static RAM on the 307-Module. This chip select is further decoded on the 307-Module to generate individual chip selects for the two banks of RAMs. Again this chip select has zero wait states inserted. RAMs as slow as 200 ns can be used but normally 100 ns or better devices are fitted.

The third chip select is used to generate the expansion bus Peripheral Address Strobe (PAS). This signal is used as part of the address decode circuits on expansion boards, simplifying interface circuits by allowing A14 downwards to be used to generate a unique address range for the peripheral rather than the whole address bus. This chip select requires an external DTACK signal to finish the cycle, which should be generated by the peripheral board.

The fourth chip select, CS3, is used on the 307-Module to select the LCD and Watch dog. This chip select also requires an external DTACK to complete the cycle.

### **2.2.4 8051 Bus**

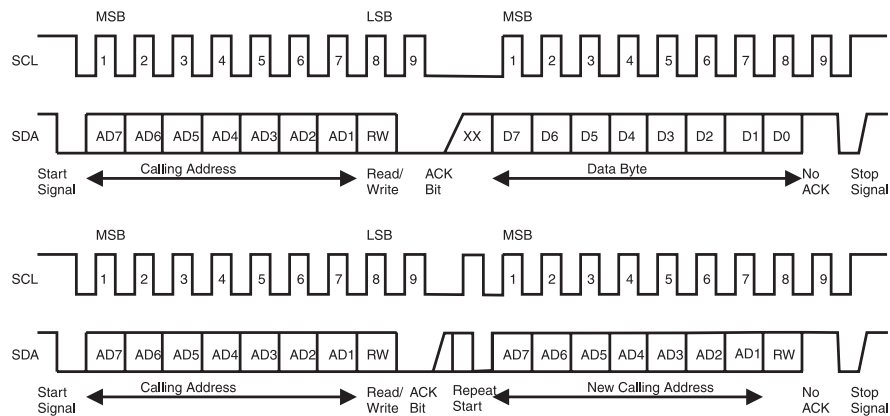
The MC68307 allows CS3 to be used optionally as an 8051 bus chip select by modifying a bit in the System Configuration Register (SCR). CS3 must also be programmed as an 8 bit bus. When this chip select is used in this way the LCD and the external watch dog will not function. The internal watch dog could be enabled to ensure that the module is running correctly. When CS3 is set to 8051 mode, to access an 8051 device all that is required is an access to an address within the range of CS3.

### **2.2.5 M-bus or I<sup>2</sup>C Bus**

The M-bus is a two wire, bi-directional serial bus which provides a simple method of exchanging data between devices. The M-bus is compatible with the I<sup>2</sup>C bus standard laid down by Philips. As the bus uses just two wires there is very little interconnection between devices on the bus. The bus is designed to operate at rates up to 100 k-bits per second with a maximum bus loading of 400 pF. The M-bus is a multi-master bus with built in arbitration and collision detection in case more than one master tries to control the bus at a time.

The M-bus uses just two wires, the serial data line (SDA) and the serial clock line (SCL), to perform all functions on the bus. All devices on the bus are connected to these signals with open collector I/O pins. Communication on the bus is made up of four parts, the start signal, the slave address transmission, the data transfer and finally the stop condition. The drawing below shows the M-bus signal descriptions.

Figure 1 M-Bus Signals



The start condition can only be sent out by a bus master. This will initiate a transfer on the bus if it is not already active. The bus is inactive if both the SDA and SCL signals are high. The start signal is defined as a high to low transition on the SDA line while SCL is high. This will wake up all slaves connected to the bus. The next piece of information to be sent by the master is the address of the slave to be accessed. This is a seven bit address with a RW bit on the end. The RW bit will inform the selected slave what type of transfer is required. The selected slave will send back an acknowledgment to the master. The acknowledge signal is sent by pulling the SDA line low during the 9th clock. If a slave does not acknowledge the master it signifies the end of the data transfer. The data transfer will now take place one byte at a time. The data word is 8 bits long and the SDA line can only be changed

while SCL is low. There is one clock pulse for each bit of data. The most significant bit is transferred first. At the end of each byte the receiver must send an acknowledge signal to the transmitter otherwise the transmission is stopped. When transmission is complete the slave must release the SDA line so that the master can issue a stop instruction by pulling the SDA line from low to high while the SCL line is high.

The MC68307 can operate either as a master or slave on the M-bus. The slave address of the MC68307 is programmed into the M-bus Address Register, enabling it to be accessed by other masters on the M-bus. More details on the M-bus can be found in the 68307 user manual section 7.

### **2.3 The UART**

The MC68307 contains a 68681 UART. The differences between the 68681 and the serial port in the microcontroller is that only one of the serial ports is used, there are no digital I/O lines and the timer can only be used to for the baud rate clock. Full details on the UART can be found in section 8 of the 68307 user manual.

The UART is configured to operate in normal full duplex asynchronous mode with RTS/CTS handshaking. The Minos operating system sets the UART up to operate at 9600 baud, 8 data bits, no parity and 1 stop bit. All these can be changed using the library code provided. A brief description of the UART registers is given in section 6.6 if required. All the serial port signals on the MC68307 are at TTL levels. The serial port drivers modify these levels to meet the specification of the serial communication standard selected.

The serial port on the 307-Module can be used with either RS-232 communications or RS-485/422 multi drop communications. See section 7.6 for link settings for these different modes.

The RS-232 serial port is configured to work with a P.C. computer. The 307-Module uses serial port buffers with charge pumps to generate the voltage levels required for RS-232 communications. This allows the 307-Module to be powered from a single 5 volt supply. When using the RS-232 serial port the 10 pin connector should be used. A 9 pin 'D' type connector can be connected to the serial port using a 10 pin IDC connector and some 10 way IDC ribbon cable. The serial port uses 4 I/O lines from the

processor, RXD, TXD, CTS and RTS. Other connections on the 9 pin 'D' connector are not supported.

The RS-485/422 can be used to network many modules together. The standard RS-485 driver has similar properties to the RS-232 serial driver. The receiver and transmitter have separate enable signals so they can be individually enabled. RS-485/422 uses differential signals making it ideal for use over long distances and in the noisy environments that are commonly found. When using RS-485/422 the 16 pin serial port connector should be used.

## **2.4 The Timer Module**

The 307-Module has two 16 bit general purpose counter timers and a software watchdog timer. Timer 1 is used by the operating system to generate the 100 Hz ticker for task switching. Full details on the timer module can be found in section 6 of the 68307 user manual.

### **2.4.1 General Purpose Timers**

Each of the general purpose timers consist of 5 registers, a timer mode register, a timer capture register, a timer count register, a reference register and an event register. The timers can be used for counting a fixed number of pulses on an input pin, counting a number of clock periods or measuring the time between events.

#### **2.4.1.1 Timer Clock Source**

There are three different clock sources for the counter timers used in timer mode.

The first is the main system clock. On the 307-Module this is 14.7456 MHz giving a maximum resolution of 67.8 ns. When using the main system clock as the timers clock source the maximum time period is 1.14 seconds, when the reference value is set to \$FFFF and the pre-scaler in the mode register is set to \$FF.

The second clock source is the system clock divided by 16. This will give a clock frequency of 921.6 kHz, a maximum resolution of 1.09  $\mu$ s and a

maximum 8.20 seconds, when the reference value is set to \$FFFF and the pre-scaler value is set to \$FF.

The third source for the clock is the timer input pin. Using this mode any time period can be set by adjusting the frequency of the source.

#### 2.4.1.2 Timer Modes

The two general purpose timers can operate in two different modes. In the first mode, the counter is incremented every clock cycle until the value in the reference value is reached. When this occurs an interrupt can be generated to carry out a special operation each timer period. Once the reference is reached the counter value can be set back to zero again or it can carry on incrementing. The following code segment will set Timer 1 up to generate interrupts at a frequency of 100 Hz.

```
tmr1    equ    $120           Timer 1 Mode Register
trr1    equ    $122           Timer 1 Reference Register
picr    equ    $24            Peripheral Interrupt Control
pivr    equ    $27            Peripheral Interrupt Vector Register

start   movea.l  #$120000,a0   Set a0 to point to base address
        ori.w    #$E888,picr(a0) Timer 1 IRQ level 6
        move.b   #$40,pivr(a0) Vector at $128
        lea     intServ(pc),a1  a1 points to interrupt service routine

        move.w   #$033B,tmr1(a0) Divide by 4, IRQ on reference
        move.w   #$9000,trr1(a0) give 100 Hz operation
```

By setting the timer clock source to the external input pin it is possible to count the number of particular transitions on the input pin.

The second mode of operation allows the timers to measure the time between two events on the timer input pin. The event can be a rising edge, a falling edge or any transition on the input pin. When the defined transition occurs the current value of the timer count register is loaded in to the timer capture register. This value can be read at any time.

### 2.4.2 Internal Watch Dog Timer

The third timer in the MC68307 is special. When this timer reaches its reference value the processor is reset. When the internal watch dog is enabled the Watch dog Reference Register (WRR) must be read before the timer times out. This is very useful feature that, when enabled, ensures that the system is running correctly all the time. On the 307-Module the internal watch dog is disabled because there is an external watch dog that can be enabled by fitting LK5.

The following code segment will enable the internal watchdog.

```
wrr    equ    $12A           Watch dog reference register
      movea.l #$120000,a0    a0 points to base address
      bset   #$0,wrr(a0)    Set the enable bit
```

The following piece of code will kick the internal watch dog to prevent it from timing out.

```
wrr    equ    $12A           Watch dog reference register
wcr    equ    $12C           Watch dog control register
      movea.l #$120000,a0    a0 points to the Base address
      move.w  #$0FFF,wrr(a0) Time out set to about 0.1 sec

main   move.w  #$FFFF,d0     Set up a delay
loop   nop
      dbra   d0,loop        loop 65536 times
      move.b #$FF,wrc(a0)   Kick the watch dog
      bra.s  main
```

## 2.5 Fast Digital I/O Lines

The MC68307 has 24 digital I/O lines. Of these 19 are used on the 307-Module, leaving 5 lines that can be used for general purpose I/O lines. Four of these lines could be used by the Timers if they are required. The spare digital I/O lines are Port A channels 3, 4 and 5 and Port B channels 6 and 7. For Minos systems these are labelled channels 128 to 132 and make up port 16 on the 307-Module. Ports 0 to 15 are I<sup>2</sup>C devices.

## 2.6 Low Power Modes

The 307-Module has several ways of reducing the current consumption of the microcontroller. Each of the modules within the microcontroller has got its own clock signal. As the microcontroller is fully static in operation these clocks can be turned off while the module is not required. When the clock is resumed the module picks up from where it left off. The table below shows the power consumption of each module in the microcontroller.

Module	Percentage I <sub>DD</sub>
All operational	100%
CLKOUT	5%
M-bus	6%
Timer	7%
UART	15%
CPU	61%
Low Power Sleep	6%

The CLKOUT signal should not be turned off when expansion boards are used since this signal provides the expansion bus clock.

If the CPU clock is turned off the CPU can be woken up again by an interrupt. The interrupt can be generated by an external source or one of the on chip peripherals providing clock to the peripheral has not been turned off. The UART can be enabled to wake the CPU when a character arrives in the

receiver even if its clock has been disabled. For a brief description of the low power mode registers see the registers section 6 . For a full description see the MC68307 user manual.

## **2.7 Registers**

Brief descriptions of the registers on the 68307 can be found in section 6 of this manual or in the 68307 user manual.

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## 3 Memory

### 3.1 Read Only Memory

The 307-Module has two 32 pin JEDEC type sockets for the read only memory. This socket can take all the standard 8 bit EPROM sizes including 27C128, 27C256, 27C512, 27C010, 27C020, 27C040 and 27C080. If the 307-Module is used with EPROMs larger than 256 k-bytes (512 k-bytes total) a different memory map must be used. Different sized EPROMs require the links on the Module to be changed, please see the EPROM links in section 7.2.

As well as taking the standard EPROMs the 307-Module can be used with Flash EPROMs up to 512 k-byte in size. The Flash EPROMs are ideal for use while developing code because they are electrically erasable in most EPROM programmers saving the time spent erasing normal EPROMs. This greatly speeds up code development. As Flash EPROMs require a 12 volt supply to program them they can not be programmed on the 307-Module. Devices supported include 28F010, 28F020 and 28F040. The link settings for Flash EPROMs and normal EPROMs are the same.

The ROM space on the 307-Module is normally mapped to the 512 k-bytes between \$000000 and \$07FFFF. Smaller devices than 512 k-bytes are reflected through this range.

The 68000 bus uses an asynchronous mode of operation. This allows the device being accessed to determine how long the cycle time is. The EPROM cycle time on the 307-Module is sufficient to allow devices as slow as 200 ns to be used.

### **3.2 Static Random Access Memory**

The standard 307-Module is fitted with 128 k-bytes of battery backed static RAM. They are in surface mounted packages placed underneath the EPROMs. The RAM is decoded between \$080000 and \$0FFFFFF. This allows for a maximum of 512 k-bytes of static RAM to be fitted to the board. The 128 k-bytes is reflected four times in this range. As the static RAM is surface mounted on the board it is not possible to change the RAM size once the board has been manufactured. 512 k-byte 307-Modules must be ordered from your distributor if that is required.

## 4 On Board Peripherals

There are a number of peripherals on the 307-Module. Some of the peripherals are memory mapped, others are connected to the microcontroller using the M-bus. For more detail on the UART please see section 8 of the 68307 user manual. For more details on the timers see section 6 of the 68307 user manual.

### 4.1 LCD Display

The 307-Module can interface to a range of LCDs that have a 4 or 8 bit direct microprocessor interface and run from a single 5 volt supply. Many suppliers including Hitachi, Varitronix, RS components etc. offer suitable displays.

All the LCDs occupy odd addresses only as standard for 8 bit devices. Although the 307-Module uses a high current buffer between the microcontroller and the LCD, the cable should be kept as short as possible.

#### 4.1.1 Alphanumeric LCDs

The 307-Module can interface directly to a number of 2 x 40 and 4 x 40 alphanumeric LCDs. Almost all the 2 line LCDs will interface directly to the 307-Module, often pins 15 and 16 on the Module LCD connector are not required for 2 line LCDs. There are a number of suitable 4 line LCDs but only the Varitronix display will plug directly into the Module. Other displays will require some connections crossing over. The LCD contrast can be adjusted using the variable resistor R15 which is next to the LCD connector.

Each two line LCD has two registers, a command/status register and a data register. From the software point of view a four line LCD is two 2 line LCDs. The LCD addresses are as follows:

Lines 1 & 2	Command	\$100001
	Data	\$100003
Lines 3 & 4	Command	\$108001
	Data	\$108003

#### 4.1.2 Graphic LCDs

The 307-Module can be used with a range of Hitachi graphics LCDs. An adapter board is required between the Module and the LCD. The graphics LCD contrast is adjusted by a variable resistor on the adapter board. The adapter board does not generate the high voltage required to drive fluorescent back lights. Graphics LCDs supported are the LMG638x series (256 x 64 pixels) and LMG640x series (240 x 128 pixels). A different driver and library code is required to use the graphics LCD effectively. Contact your distributor for full details.

#### 4.1.3 Vacuum Fluorescent Displays

Some vacuum fluorescent displays can be used with the 307-Module but an adapter board is required. Different driver code and programmable device will also be required from that usually distributed with the 307-Module. Please contact your distributor for full details.

### 4.2 The External Watch dog

The external watch dog can be used to keep an eye on the system. Once the watch dog is enabled by fitting LK5, a register must be accessed periodically to prevent the watch dog timing out. If the watch dog times out it will reset the system. The external watch dog time out is set to about 360 ms. There is also a watch dog built in to the MC68307. This internal watch dog is disabled during normal operation. A visual indication of the watch dog is given by the green LED D4. This LED is connected to the watch dog trigger which means that it can be used as an effective indicator even if the watch dog link is not fitted.

The external watch dog has two registers associated with it. They are:

Watch dog set    \$110001

Watch dog clear \$118001

Functions are provided by the Minos operating system to toggle the watch dog.

## 4.3 Digital I/O

### 4.3.1 I<sup>2</sup>C bus (M-bus) Digital I/O

Most of the digital I/O lines on the 307-Module are provided by four M-bus I/O ports. Each of these provides 8 quasi bi-directional lines with change of state recognition on each line. The I<sup>2</sup>C bus (M-bus) ID numbers have been set as follows.

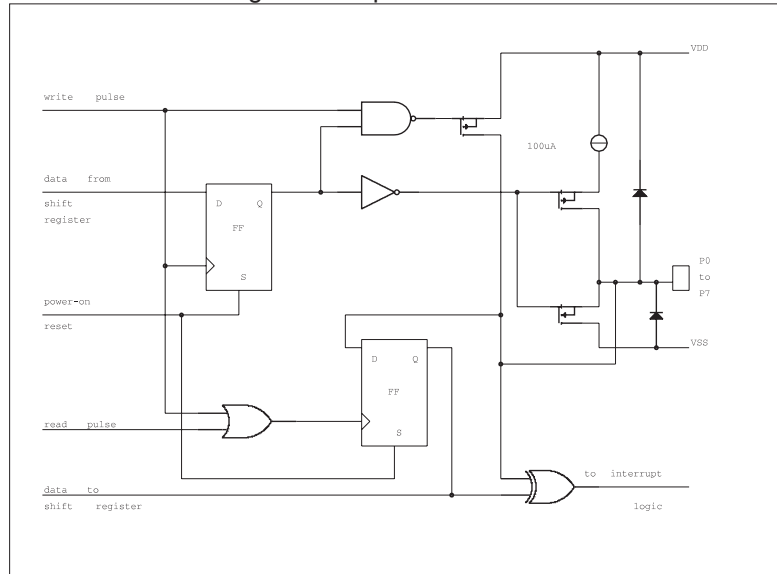
Port	ID Number	Read Address	Write Address
0	\$20	\$41	\$40
1	\$21	\$43	\$42
2	\$22	\$45	\$44
3	\$23	\$47	\$46

The figure below shows a simplified circuit for the output driver for each channel. The high level is provided by a 100  $\mu$ A current source which will easily drive a LS TTL input. It also means that in input mode the I/O lines will read back as high even if nothing is connected. The low level output is provided by a high current FET which can sink an input current of 25 mA making it ideal for driving LEDs or the CMS range of digital signal conditioning cards.

#### 4.3.1.1 Direction Control

There is no direct control over the direction of each of the I/O pins. They are always outputs, but since the high level is provided by a current source it is safe to drive into the I/O line as long as it is high at the time. When a port is read the data reflects the actual state of the pins not the data which was last written. When writing to the ports it is worth using a mask to prevent any lines from being set low while they are being used as inputs.

Figure 2 Output Driver Circuit



#### 4.3.1.2 Interrupts

Each of the ports has a change of state detector inside it which constantly compares the state of the pins with a copy of the state of the pins when the port was last read. If there is a difference an interrupt is generated. The interrupt is removed when either the port returns to its original state or when the port is read. The interrupts from the ports can be enabled or disabled by writing to the appropriate latched interrupt register (see the registers section 6). There is no need to check to see if the port was responsible for the interrupt because there is only one device on each of the interrupt lines.

Port 0	interrupts on INT5
Port 1	Interrupts on INT6
Port 2	Interrupts on INT1
Port 3	Interrupts on INT1

Ports 2 & 3 both use INT1 which makes the keypad scanning easier but it means that both ports may need to be read to determine which one is responsible for a particular interrupt.

#### **4.3.2 CPU Digital I/O**

The 307-Module has 5 digital I/O lines that are spare on the microcontroller. These I/O lines can be used as general purpose I/O lines or for a special function. The spare I/O lines are Timer 1 In, Timer 2 In, Timer 1 Out, Timer 2 Out and PA5. These signals can not generate interrupts but they can be scanned much faster than those used on the M-bus. All the other I/O lines from the microcontroller have been used for special functions on the 307-Module and should not be used for general purpose I/O lines.

## 4.4 Analogue I/O

The analogue I/O on the 307-Module is provided by an I<sup>2</sup>C bus (M-bus) 8-bit data acquisition device. The I<sup>2</sup>C bus (M-bus) ID for the device is:

ID Number	Read Address	Write Address
\$48	\$91	\$90

### 4.4.1 Analogue Reference

The voltage range of the ADC and DAC is controlled by the on board precision reference which can be adjusted using the variable resistor R1. The reference voltage is set to 2.560 Volts during factory testing which gives an input and output voltage range of 0 to 2.55 Volts or 10 mV per bit.

### 4.4.2 Analogue Inputs

The analogue inputs are sampled using an 8 bit successive approximation analogue to digital converter. The A to D also includes a sample and hold amplifier and a multiplexer which allows four single ended inputs, three quasi differential inputs or two differential inputs.

#### 4.4.2.1 Single Ended

This is the simplest mode and has four channels. Each input should be connected to the corresponding +ve input on the I/O connector. The voltage is measured between the input and analogue ground. This method works well on short cables in low noise environments but is prone to voltage drops in long cables.

#### 4.4.2.2 Differential

This mode is ideal for noisy environments as it measures the difference between two inputs. Any noise which is induced in the cables is canceled out at the input amplifier. There are only two channels available in this mode and connections should be made to the +ve and -ve inputs. The common mode voltage and noise can be further reduced by using shielded cables and

connecting the shield to the analogue grounds on the 307-Module and the equipment.

#### **4.4.2.3 Quasi Differential**

This mode offers the advantage of noise immunity but allows three separate channels to be used by connecting the -ve inputs of the three channels to one input. Connections should be made by connecting the inverting outputs of the equipment to Adc1 -ve and the non inverting inputs to Adc1, 2 and 3 +ve.

#### **4.4.3 Analogue Output**

The analogue output is generated using an 8 bit multiplying DAC. This is part of the data acquisition chip.

### **4.5 Real Time Clock**

The Real Time Clock provides a clock and calendar down to 1/100 second, a timer which will count up to 99 days and an alarm which can generate an interrupt at a particular time and date in the clock or timer. The clock will cause interrupts on INT2. The clock device used is an I<sup>2</sup>C bus (M-bus) device but it is not connected to the M-bus on the 307-Module. The real time clock occupies the same address as most EEPROMs that can be used on the M-bus. To enable these devices to be connected to the bus it was decided to connect the real time clock to the processor using two general purpose I/O lines.

Data is stored in the Real Time Clock in BCD format i.e. four bits in each register are used to store each digit.

The clock contains a two bit year counter which can be used to increment a separate year register (possibly kept in the spare RAM in the clock). Each time the clock is read the years counter must be compared with the RAM copy of its value the last time the clock was read. If the counter has changed then the years counter in the RAM should be incremented accordingly. If the years counter is initialized to the number of years since the last leap year then year 0 will have a 29th February. This does of course mean that the clock must be read at least once every four years.



## 5 Module Bus expansion

### 5.1 Introduction

The 307-Module uses the Module Bus expansion to enable it to interface to a wide range of peripheral boards including graphics displays, serial communications, digital I/O ports, analogue I/O ports, printer ports etc.. This section of the manual describes the working of the bus and suggests some methods of interfacing to it.

The Module Bus uses three basic modes of operation, 68000 peripherals, 68000 memory and 8051 peripherals. Each mode uses the same address and data bus but a different set of control lines. The Module Bus also supports five interrupt lines, four of which are maskable.

### 5.2 Bus Width Considerations

The 68000 memory and peripheral modes both use the full 16 bit data bus on the 68000. This means that as the address increases bytes are read alternatively from D8-D15 and D0-D7. This is not a problem with memory as two 8 bit devices can be used, one for each half of the data bus. However peripheral devices which have only 8 bit data busses must multiplex between D8-D15 and D0-D7. The simplest, and most common, solution is to connect the peripheral to D0-D7 and connect A1 on the bus to A0 on the peripheral etc.. This offset in the address lines mean that the peripheral will only be accessible at alternate addresses. Using D0-D7 means that the registers are accessible on odd addresses only and gives a degree of compatibility with 68000 systems which also use D0-D7 for interrupt vector fetches. The 68000 instruction set has a group of instructions (movep) which are designed to read and write multiple bytes to peripheral devices connected in this way. On the 307-Module it is possible to program the expansion bus to be an 8 bit cycle. This is not recommended for compatibility because, when using the 8 bit bus width of the MC68307, the peripheral must be connected to the UPPER D8-D15 data lines not the lower D0-D7 as with standard 68000 bus peripheral cycles.

### **5.3 Asynchronous Operation**

The 68000 bus uses an asynchronous mode of operation to access peripherals and memory. This means that the speed of each bus cycle is determined dynamically during each bus cycle. The processor starts a bus cycle by supplying the address and data followed by some control signals to say that they are valid. The participating peripheral must then wait until it has accepted the CPU's data (write cycle) or provided data for the CPU (read cycle) before asserting the DTACK (data transfer acknowledge) signal to tell the CPU to complete the cycle.

The 307-Module can generate the DTACK internally after a programmed number of wait states after a chip select has been asserted if required. This is not recommended, and is not used on Minos systems, when accessing the Module Bus peripherals as all expansion boards on the bus will generate their own DTACK signal when they are ready.

### **5.4 Memory Expansion**

The memory expansion mode is used to add large blocks of external memory to the Module Bus. In this mode all the external Module Bus address lines must be decoded and the MAS signal should be used to enable the decoders. The memory may be read or written 8 or 16 bits at a time with the size controlled by the DS0 and DS1 signals. If DS0 only is asserted then a data byte is to be transferred on D0 to D7 only. If DS1 is asserted on its own then the data byte is transferred on D8 to D15. If both DS0 and DS1 are asserted at the same time then it is a 16 bit transfer with all data lines used. A simple OR gate and inverter can be used with DS0, DS1 and Write to produce separate strobe lines for the two halves of the data bus. Figure 3 shows this circuit.

Figure 3 Read and Write Strobes

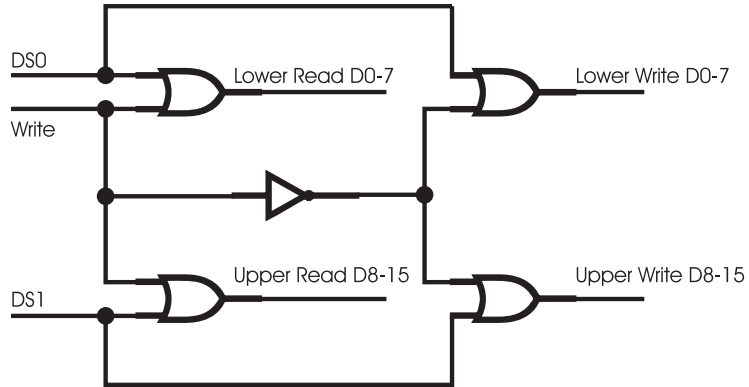


Figure 4 and figure 5 are timing diagrams for 68000 read and write cycles.

Figure 4 Module Bus Read Cycle

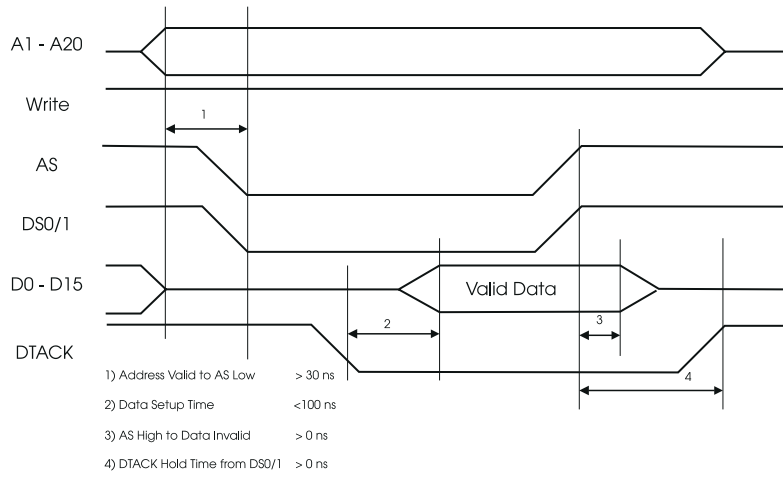
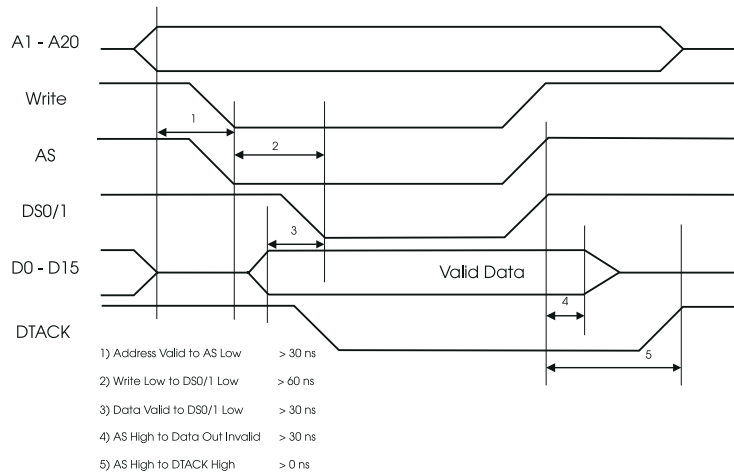


Figure 5 Module Bus Write Cycle



## 5.5 Peripheral Expansion

The peripheral expansion mode is used to add I/O devices to the 68000 bus. Transfers can be made in 8 or 16 bits but if 8 bit devices are used they should be connected to D0 - D7 and should have the address lines offset (see Bus Width Considerations). The address decoding only needs to include A14 downwards and the decoder should be enabled with the PAS signal.

## 5.6 Interrupts

The Module Bus includes a number of interrupt inputs which can be used freely by expansion boards. Three of the lines correspond to levels 3, 4 and 7. The other line is the non maskable interrupt and will always generate an interrupt level 7. The interrupt lines are edge sensitive and should be driven with open collector drivers. They are pulled up on the controller board.

## 6 Registers

### 6.1 Introduction

This section contains a list of all the registers in the 68307. It gives a brief description of the function of the register. More information can be found in the 68307 user manual (page numbers for the 68307 user manual are given in the tables below).

#### System Configuration Registers

Address	Register Name		Page
\$0000F0	Reserved		
\$0000F2	Module Base Address Register	MBAR	5-22
\$0000F4	System Control Register high word	SCRh	5-23
\$0000F6	System Control Register low word	SCRI	5-23
\$0000F8	Reserved		
\$0000FA	Reserved		
\$0000FC	Reserved		
\$0000FE	Reserved		

Note-The addresses given below depend on the base address in MBAR

#### External Bus Interface Registers

Address	Register Name		Page
\$120011	Port A Control Register	PACNT	5-34
\$120013	Port A Data Direction Register	PADDR	5-35
\$120015	Port A Data Register	PADAT	5-35
\$120016	Port B Control Register	PBCNT	5-36
\$120018	Port B Data Direction Register	PBDDR	5-36
\$12001A	Port B Data Register	PBDAT	5-37

## Interrupt Control Registers

Address	Register Name		Page
\$120020	Latched Interrupt Control Register 1	LICR1	5-38
\$120022	Latched Interrupt Control Register 2	LICR2	5-38
\$120024	Peripheral Interrupt Control Register	PICR	5-39
\$120027	Programmable Interrupt Vector Register	PIVR	5-40

## Chip Select Registers

Address	Register Name		Page
\$120040	Base Register 0	BR0	5-30
\$120042	Option Register 0	OR0	5-32
\$120044	Base Register 1	BR1	5-30
\$120046	Option Register 1	OR1	5-32
\$120048	Base Register 2	BR2	5-30
\$12004A	Option Register 2	OR2	5-32
\$12004C	Base Register 3	BR3	5-30
\$12004E	Option Register 3	OR3	5-32

## UART Registers

Address	Register Name		Page
\$120101	UART Mode Register 1	UMR1	8-15
\$120101	UART Mode Register 2	UMR2	8-17
\$120103	UART Status Register (read)	USR	8-19
\$120103	UART Clock Select Register (write)	UCSR	8-21
\$120105	UART Command Register (write)	UCR	8-23
\$120107	UART Receiver Buffer (read)	URB	8-25
\$120107	UART Transmitter Buffer (write)	UTB	8-25
\$120109	UART Input Port Change Register (read)	UIPCR	8-26

---

Address	Register Name		Page
\$120109	UART Auxiliary Control Register (write)	UACR	5-26
\$12010B	UART Interrupt Status Register (read)	UISR	5-27
\$12010B	UART Interrupt Mask Register (write)	UIMR	5-28
\$12010D	UART Baud Rate Pre-scaler high byte	UBG1	5-29
\$12010F	UART Baud Rate Pre-scaler low byte	UBG2	5-29
\$120119	UART Interrupt Vector Register	UIVR	5-29
\$12011B	UART Input Port Register (read)	UIP	5-29
\$12011D	UART Output Port Data Register 1 (write)	UOP1	5-30
\$12011F	UART Output Port Data Register 0 (write)	UOP0	5-30

#### Timer Module Registers

Address	Register Name		Page
\$120120	Timer 1 Mode Register	TMR1	6-4
\$120122	Timer 1 Reference Register	TRR1	6-5
\$120124	Timer 1 Capture Register	TCR1	6-5
\$120126	Timer 1 Counter	TCN1	6-5
\$120129	Timer 1 Event Register	TER1	6-6
\$12012A	Watch dog Reference Register	WRR	6-7
\$12012C	Watch dog Counter Register	WCR	6-7
\$120130	Timer 2 Mode Register	TMR2	6-4
\$120132	Timer 2 Reference Register	TRR2	6-5
\$120134	Timer 2 Capture Register	TCR2	6-5
\$120136	Timer 2 Counter	TCN2	6-5
\$120139	Timer 2 Event Register	TER2	6-6

I<sup>2</sup>C bus (M-Bus) Module Registers

Address	Register Name		Page
\$120141	M-Bus Address Register	MADR	7-6
\$120143	M-Bus Frequency Divider	MFDR	7-6
\$120145	M-Bus Control Register	MBCR	7-7
\$120147	M-Bus Status Register	MBSR	7-9
\$120149	M-Bus Data I/O Register	MBDR	7-10

Please note that the addresses given refer to the most significant byte of the register. For 32 bit registers this will be bits 31 to 24, for 16 bit registers this will be bits 15 to 8.

## 6.2 System Configuration Registers

### Module Base Address Register

**\$0000F2**

FC2	FC1	FC0	CFC	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----

This register contains the address and function codes to enable the CPU to address the on chip peripherals. It can only be accessed in supervisor mode. The upper 12 address lines are used to decode the position of the registers in the memory map. By setting the compare function code bit the on chip peripherals can only be accessed in the defined function codes. The function code for the 68000 interrupt acknowledge cycle should never be programmed into this register. For full details see page 5-22 in the 68307 user manual.

- FC2 - 0    Function Codes
- CFC       Compare Function Codes - If set then function codes are used
- A23 -12   Defines the base address for the registers

On a Minos system this register is programmed with the value \$0120 to give the base address \$120000, function codes are ignored.

### System Control Register (SCR)

**\$0000F4**

ADC	WPV	HWT		RS1	RS0			ADCE	WPVE	EPCS	E8051	BUS W0	BUS W1	BUS W2	BUS W3
HWDE	HW2	HW1	HW0	UACW	UACD	TMCD	MBCD	LPEN	CDEN	CKD	EBU SW		CD2	CD1	CD0

This 32-bit register describes how the system is set up. It can be read or written at any time, in either byte, word or long word accesses. The top 8 bits, when read, will reveal the status of the system. The remaining 24-bits are used to configure the micro-controller. This register can only be accessed in supervisor mode. After a reset the status bits are set to 0. An occurrence of the relevant event will set the bit. A bit can be cleared by writing a 1 to the appropriate bit. In the 68307 user manual (page 5-23) most of the time periods given are for a clock speed of 16.67 MHz. The 307-Module is clocked at 14.7456 MHz and so times should be recalculated accordingly. Note that the 68000 stores the most significant byte first i.e. the byte at address \$F4 will access the first byte, \$F5 accesses the second byte (ADCE - BUSW3), \$F6 byte HWDE to MBCD etc.

Status bits

ADC Address Decode Conflict  
WPV Write Protection Violation  
HWT Hardware Watch dog Time out (Bus Error)  
RS1 - 0 Reset Source- gives the cause of the last reset

Control bits

ADCE Address Decode Conflict Enable- generates BERR  
WPVE Write Protect Violation Enable - generates BERR  
EPCS Enable Peripheral Chip Selects - divides CS2 into four  
E8051 Enable 8051 bus  
BUSW0 Bus Width 0 - size of data bus for CS0  
BUSW1 Bus Width 1 - size of data bus for CS1  
BUSW2 Bus Width 2 - size of data bus for CS2  
BUSW3 Bus Width 3 - size of data bus for CS3  
HWDE Hardware Watch dog Enable - enables the BERR timer  
HW2 - 0 Hardware Watch dog Count - sets the time period for BERR  
UACW UART Clock Wake up - allows UART clock to start when a character is received  
UACD UART Clock Disable - turns the UART module clock off  
TMCD Timer Clock Disable - turns the Timer module clock off  
MBCD I<sup>2</sup>C bus (M-Bus) Clock Disable - turns the M-Bus clock off  
LPEN Low Power Enable - enables low power modes  
CKD Clock Output Disable - turns the CLKOUT signal off  
EBUSW Enable Bus Width - determines bus width for non chip-select devices  
LPCD2 -0 Low Power Clock Divider set the clock speed if LPEN is set

### 6.3 I/O Port Control Registers

#### Port A Control Register (PACNT)

**\$120011**

CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
-----	-----	-----	-----	-----	-----	-----	-----

This register is used to specify the function of the I/O port A. Each of the I/O pins making up port A has two functions. They can either be a dedicated special function pin or a general purpose I/O pin. To configure any of the port A pins to function as their special I/O function set the required bit in this register. To enable this port to function as general purpose I/O port, clear the bits in this register. Full details can be found on page 5-34 of the 68307 user manual. The table on page 5-12 of the 68307 User Manual shows the alternative function of each of the Port A I/O line.

#### Port A Data Direction Register (PADDR)

**\$120013**

DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
-----	-----	-----	-----	-----	-----	-----	-----

This 8-bit register is used to set the direction of each of the port A lines. By setting a bit in this register the associated port A line is configured as an output. On reset this register is cleared and so all the port A pins will function as inputs. Full details can be found on page 5-35 of the 68307 user manual.

#### Port A Data Register (PADAT)

**\$120015**

PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
-----	-----	-----	-----	-----	-----	-----	-----

This 8-bit register is used to store the logic states of the port A lines. When the port is configured as outputs a logic zero will be output on all the port A lines unless the data register is configured before the direction is changed. In output mode this register stores the value output on the port a lines, in input mode this register is read to input the value of the port A lines. At reset all the bits in this register are 0. Full details of this register can be found on page 5-35 of the 68307 user manual.

**Port B Control Register (PBCNT)****\$120016**

CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
------	------	------	------	------	------	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----

This 16-bit register is used to specify the function of the I/O port B. Each of the I/O pins making up port B has two functions. They can either be a dedicated special function pin or a general purpose I/O pin. To configure any of the port B pins to function as their special I/O function set the required bit in this register. To enable this port to function as general purpose I/O port, clear the bits in this register. Full details of this register can be found on page 5-36 of the 68307 user manual. The table on page 5-12 of the 68307 User Manual shows the alternative function of each Port B I/O line.

**Port B Data Direction Register (PBDDR)****\$120018**

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
------	------	------	------	------	------	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----

This 16-bit register is used to set the direction of each of the port B lines. By setting a bit in this register the associated port B line is configured as an output. On reset this register is cleared and so all the port B pins will function as inputs. Further details on this register can be found on page 5-36 of the 68307 user manual.

**Port B Data Register (PBDAT)****\$12001A**

PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
------	------	------	------	------	------	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----

This 16-bit register is used to store the logic states of the port B lines. When the port is configured as outputs a logic zero will be output on all the port B lines unless the data register is configured before the direction is changed. In output mode this register stores the value output on the port a lines, in input mode this register is read to input the value of the port B lines. At reset all the bits in this register are reset to zero. More details on this register can be found on page 5-37 of the 68307 user manual.

## 6.4 Interrupt Control Registers

### Latched Interrupt Control Register (LICR)

\$120020

PIR1	INT1L2	INT1L1	INT1L0	PIR2	INT2L2	INT2L1	INT2L0	PIR3	INT3L2	INT3L1	INT3L0	PIR4	INT4L2	INT4L1	INT4L0
PIR5	INT5L2	INT5L1	INT5L0	PIR6	INT6L2	INT6L1	INT6L0	PIR7	INT7L2	INT7L1	INT7L0	PIR8	INT8L2	INT8L1	INT8L0

This 32-bit register is used to control the interrupt priorities of the 8 general purpose interrupt inputs (alternative function for Port B8-15). Each of the 8 interrupt lines has four bits assigned to it in these registers. One of the bits is a interrupt reset bit which allows the software to clear a pending interrupt. Writing a 1 to the reset bit will clear the interrupt latch. The other three bits for each input is the priority level between 0 and 7. If the level is programmed as 0 the interrupt is disabled. Level 7 is the highest priority. Full details can be found on page 5-38 of the 68307 user manual.

Note: the 68000 stores its registers most significant byte first i.e. \$120020 accesses the byte PIR1 to INT2L0, \$120021 PIR3 to INT4L0 etc.

PIR8 - 1 Pending Interrupt reset - clears a latched interrupt on the relevant interrupt input pin

INT1L2 - 0 Interrupt Level - allow programming the interrupt level for INT1

INT2L2 - 0 Interrupt Level - allow programming the interrupt level for INT2

INT3L2 - 0 Interrupt Level - allow programming the interrupt level for INT3

INT4L2 - 0 Interrupt Level - allow programming the interrupt level for INT4

INT5L2 - 0 Interrupt Level - allow programming the interrupt level for INT5

INT6L2 - 0 Interrupt Level - allow programming the interrupt level for INT6

INT7L2 - 0 Interrupt Level - allow programming the interrupt level for INT7

INT8L2 - 0 Interrupt Level - allow programming the interrupt level for INT8

**Peripheral Interrupt Control Register (PICR)****\$120024**

PI_T1	T1L2	T1L1	T1L0	PI_T2	T2L2	T2L1	T2L0	PI_UA	UAL2	UAL1	UAL0	PI_MB	MBL2	MBL1	MBL0
-------	------	------	------	-------	------	------	------	-------	------	------	------	-------	------	------	------

This 16-bit register is used to set up the interrupt levels generated by the on chip peripherals. For each of the four on chip interrupt sources there are four bits in this register. The value placed in three of these bits will determine the interrupt level for that peripheral. The fourth bit, when read will determine whether the peripheral has an interrupt pending. Writing will not affect this fourth bit. This fourth bit is defined in the errata to the user manual, the rest of the register is described on page 5-39 of the 68307 user manual.

PI_T1	Pending interrupt on T1 if this bit is set
T1L2 - 0	Interrupt level for T1 - used for 100 Hz Timer on 307-Module
PI_T2	Pending interrupt on T2 if this bit is set
T2L2 - 0	Interrupt level for T2 - used for 100 Hz Timer on 307-Module
PI_UA	Pending interrupt on UART module if this bit is set
UAL2 - 0	Interrupt level for the UART module
PI_MB	Pending interrupt for the M-Bus module
MBL2 - 0	Interrupt level for M-Bus module

**Programmable Interrupt Vector Register (PIVR)****\$120027**

IV7	IV6	IV5	IV4				
-----	-----	-----	-----	--	--	--	--

This register is used to specify the vector numbers that are returned by the interrupt controller in response to an IACK cycle for the different peripherals. The top four bits are programmed into this register, the lower four bits is provided by the interrupt controller for a specific interrupt level. See page 5-16 of the 68307 User Manual for a list of all the vector numbers that are generated by the interrupt controller for each interrupt source. Further details of this register can be found on page 5-40 of the 68307 user manual.

On Minos systems this register is programmed as \$40. To get the vector number the value \$40 is added to the number given above for the particular peripheral. This value is then multiplied by 4 to give an address for the service routine.

## 6.5 Chip Select Registers

For each of the four chip select lines that are generated by the MC68307, there are two 16-bit registers. The base address register and the option register. These registers may be written to individually or at the same time using as a long write which may be better in some cases.

If two or more chip select lines are programmed for the same address then an Address Decode Conflict will occur, setting the ADC bit in the top part of the system configuration register. A bus error can be generated if it is enabled. The chip select logic of the 68307 will prevent two chip select lines going low at the same time by implementing a priority system. CS0 has the highest priority while CS3 has the lowest.

### Base Register 0 (BR0)

**\$120040**

FC2	FC1	FC0	BA23	BA22	BA21	BA20	BA19	BA18	BA17	BA16	BA15	BA14	BA13	RW	EN
-----	-----	-----	------	------	------	------	------	------	------	------	------	------	------	----	----

This register contains the base address of the EPROM on the 307-Module and any function codes that need to be compared before the EPROM is chip selected. Also contained in this register is a read or write only bit and an enable bit.

- FC2 - 0    Function code for the chip select if enabled
- BA23 - 13    Base address for chip select 0
- RW        Defines the type of access if MRW bit is set in option register
- EN        Enables the chip select line

Full details on the base registers can be found on page 5-30 of the 68307 user manual.

**Option Register 0 (OR0)****\$120042**

DTK2	DTK1	DTK0	M23	M22	M21	M20	M19	M18	M17	M16	M15	M14	M13	MRW	CFC
------	------	------	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----

This register is used to set the number of wait states for the EPROM and the size of the block that the EPROM occupies.

- DTK2 - 0 DTACK delay - defines the delay time for DTACK.  
M23-M13 Base Address Mask - defines the size of the chip select  
MRW Mask RW bit - this allows Read or Write access only in conjunction with the RW bit in the Base Register  
CFC Compare Function Codes - enables the function code comparison

Full details on the option registers can be found on page 5-32 of the 68307 user manual.

**Base Register 1 (BR1)****\$120044**

This register is used to select the base address of the RAM on the 307-Module. For a full description of this register see Base Register 0.

**Option Register 1 (OR1)****\$120046**

This register determines the size of the block for the RAM chip select and the number of wait states to be inserted before the DTACK signal is generated. For a description of this register see Option Register 0.

**Base Register 2 (BR2)****\$120048**

This register is used to select the base address of chip select 2 on the 307-Module. This is used to decode the peripheral address space (PAS). For a full description of this register see Base Register 0.

**Option Register 2 (OR2)****\$12004A**

This register determines the size of the block for chip select 2 and the number of wait states to be inserted before the DTACK signal is generated. For a description of this register see Option Register 0.

**Base Register 3 (BR3)****\$12004C**

This register is used to select the base address of chip select 3 on the 307-Module. For a full description of this register see Base Register 0. This chip select is used to decode the watchdog, LCD and memory address strobe (MAS).

**Option Register 3 (OR3)****\$12004E**

This register determines the size of the block for chip select 3 and the number of wait states to be inserted before the DTACK signal is generated. For a description of this register see Option Register 0.

**6.6 UART Registers**

Full details on the UART registers and programming can be found in the 68681 data sheet or section 8 of the 68307 user manual, details in the Appendix. The 68307 user manual refers to timings obtained using 16.67 MHz or 3.6864 MHz clock speed. The 307-Module is clocked at 14.7456 MHz, this should be taken into account when calculating baud rates etc.

**Mode Register 1 (UMR1)****\$120101**

RxRTS	RxIRQ	ERR	PM1	PM0	PT	BC1	BC0
-------	-------	-----	-----	-----	----	-----	-----

This register controls some of the serial port configuration. At reset this register is cleared to 0. Full details on this register can be found on page 8-15 of the 68307 user manual.

RxRTS	enables control of data flow using RTS
RxIRQ	determines the source of the receiver interrupt
ERR	controls the function of the RB, FE & PE bits in the status register (USR)
PM1 -0	defines the parity mode for the serial port
PT	used to define the parity type
BC1 - 0	sets the number of bits per character between five and eight

**Mode Register 2 (UMR2)****\$120101**

CM1	CM0	TxRTS	TxCTS	SB3	SB2	SB1	SB0
-----	-----	-------	-------	-----	-----	-----	-----

This register contains some more set up bits for the serial port. It is accessed immediately after the UMR1 is accessed. At reset all the bits in this register are cleared. Full details on this register can be found on page 8-17 in the 68307 user manual.

- CM1 - 0 set the communication mode
- TxRTS controls the RTS signal
- TxCTS enables data flow control using CTS
- SB3 - 0 determines the number of stop bits

**UART Status Register (USR)****\$120103**

RB	FE	PE	OE	TxEMP	TxRDY	FFULL	Rx RDY
----	----	----	----	-------	-------	-------	-----------

This read only register is used to return the status of the serial port. At reset all the values are set to 0. Full details can be found on page 8-19 of the 68307 user manual.

- RB set if a break character has been received
- FE set if no stop bit was received after a character (framing error)
- PE set if a parity error has occurred
- OE set if one or more characters have been lost due to the buffer being full
- TxEMP set if after transmission of the last stop bit , there are no characters in the transmitter buffer.
- TxRDY set if the transmitter buffer is empty and ready to be loaded
- FFULL set if a character has been received and is in the receiver buffer waiting to be read. Up to 2 characters could be in the buffer
- Bit 0 set if one or more characters are waiting to be read

**UART Clock Select Register (UCSR)****\$120103**

RCS3	RCS2	RCS1	RCS0	TCS3	TCS2	TCS1	TCS0
------	------	------	------	------	------	------	------

This write only register selects the baud rate clocks for both the receiver and the transmitter. There are two sets of baud rates. Set 1 is selected if bit 7 in UACR is cleared and set 2 is selected if this bit is set. Full details can be found on page 8-21 of the 68307 user manual. Note that the 307-Module serial port is clocked at 14.7456 MHz so baud rates will be four times those shown in the tables in the user manual.

RCS3 - 0 Receiver baud rate select

TCS3 - 0 Transmitter baud rate select

**UART Command Register (UCR)****\$120105**

	MISC2	MISC1	MISC0	TC1	TC0	RC1	RC0
--	-------	-------	-------	-----	-----	-----	-----

This write only register is used to pass commands to the UART. Multiple commands can be given if they are non conflicting. Full details can be found on page 8-23 of the 68307 user manual.

MISC2 - 0 select an individual command

TC1 - 0 reset the transmitter

RC1 - 0 reset the receiver

**Receiver Buffer (URB)****\$120107**

RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
-----	-----	-----	-----	-----	-----	-----	-----

This eight bit read only register contains the character in the receiver buffer. At reset this register is cleared to zero. Details of this register can be found on page 8-25 of the 68307 user manual.

**Transmitter Buffer (UTB)****\$120107**

TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
-----	-----	-----	-----	-----	-----	-----	-----

This eight bit write only register contains the character about to be transmitted. At reset this register is cleared to zero. Full details are on page 8-25 of the 68307 user manual.

**Input Port Change Register (UIPCR)****\$120109**

			COS				CTS
--	--	--	-----	--	--	--	-----

This read only register shows the current state of the CTS input pin. At reset it is cleared to zero. Only two bits have any meaning, all others are reserved. Full details can be found on page 8-26 of the 68307 user manual.

- COS      set if a change of state lasting longer than 25 - 50 $\mu$ s on the CTS input has occurred  
 CTS      reflects the current state of the CTS input pin

**Auxiliary Control Register (UACR)****\$120109**

BRG	CTM S2	CTM S1	CTM S0				IEC
-----	-----------	-----------	-----------	--	--	--	-----

This write only register selects which baud rate set is used and controls the receiver and transmitter handshaking. At reset this register is cleared to zero. Full details can be found on page 8-26 of the 68307 user manual.

- BRG      if this bit is set then baud rate set 2 is used otherwise set 1 is used.  
 CTMS2   must be set  
 CTMS1   must be clear  
 CTMS0   must be clear  
 IEC      if set then a change of state on CTS will generate an interrupt

**Interrupt Status Register (UISR)****\$12010B**

COS					DB	Rx RDY	TxRDY
-----	--	--	--	--	----	-----------	-------

This read only register gives the status of all potential interrupt sources on the UART. This register is masked by the UIMR before an interrupt will be generated. Details on page 8-27 of the 68307 user manual.

- COS      if set then a change of state has occurred on CTS and caused an interrupt  
 DB      either the beginning or end of a break has been detected  
 RxRDY   either FFULL or RxRDY depending on setting in UMR1  
 TxRDY   this bit is a duplication of the TxRDY bit in the USR.

**Interrupt Mask Register (UIMR)****\$12010B**

COS					DB	Rx RDY	TxRDY
-----	--	--	--	--	----	-----------	-------

This write only register is used to enable or disable a particular interrupt source. If the relevant bit in this register is set and the same bit in the UISR is set then an interrupt will be generated. Full details can be found on page 8-28 of the 68307 user manual.

**Timer Upper Preload Register (UBG1)****\$12010D**

This eight bit write only register holds the 8 most significant bits of the preload value to be used by the timer in order to provide the required baud rate. Details can be found on page 8-29 of the 68307 user manual.

**Timer Lower Preload Register (UBG2)****\$12010F**

This eight bit write only register holds the 8 least significant bits of the preload value to be used by the timer in order to provide the required baud rate. Details can be found on page 8-29 of the 68307 user manual.

**Interrupt Vector Register (UIVR)****\$120119**

IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
------	------	------	------	------	------	------	------

This eight bit register contains the vector register for the UART interrupt vector fetches. It contains an offset from the base of the vector table where the address for the exception handler can be found. Full details can be found on page 8-29 of the 68307 user manual.

**Input Port Register (UIP)****\$12011B**

							CTS
--	--	--	--	--	--	--	-----

This read only register gives the current state of the CTS input pin. At reset this register is set to \$FF. Only one bit is defined in this register, all others are reserved. Details can be found on page 8-29 of the 68307 user manual.

CTS      Change the state of the CTS line





**Watch dog Reference Register (WRR)****\$12012A**

REF15	REF14	REF13	REF12	REF11	REF10	REF9	REF8	REF7	REF6	REF5	REF4	REF3	REF2	REF1	EN
-------	-------	-------	-------	-------	-------	------	------	------	------	------	------	------	------	------	----

This register contains the reference value for the watch dog timer. At reset this register is set to \$FFFF enabling the watch dog with its maximum time out period. If the watch dog counter reaches the value contained in this register the micro-controller will be reset. Full details can be found on page 6-7 of the user manual.

REF15 - 1 watch dog time out counter value.

EN when set this enables the watch dog internal watchdog. This is disabled on the 307-Module as there is an external watchdog provided by the MAX691.

**Watch dog Counter Register (WCR)****\$12012C**

This register contains the current value of the watch dog counter. This register must be written to periodically to prevent the system being reset by the watch dog. Full details on this register can be found on page 6-7 in the 68307 user manual.

**Timer 2 Mode Register (TMR2)****\$120130**

This is the timer 2 mode register. For a description of how to set this register up see Timer 1 Mode Register.

**Timer 2 Reference Register (TRR2)****\$120132**

This is the timer 2 reference register. For a description of how to set this register up see Timer 1 Reference Register.

**Timer 2 Capture Register (TCR2)****\$120134**

This is the timer 2 capture register. For a description of how to set this register up see Timer 1 Capture Register.

**Timer 2 Count Register (TCN2) \$120136**

This is the timer 2 count register. For a description of how to set this register up see Timer 1 Count Register.

**Timer 2 Event Register (TER2) \$120139**

This is the timer 2 event register. For a description of how to set this register up see Timer 1 Event Register.

**6.8 I<sup>2</sup>C bus (M-Bus) Module Registers**

Full descriptions of the I<sup>2</sup>C bus (M-Bus) module can be found in section 7 of the 68307 user manual.

**I<sup>2</sup>C bus (M-Bus) Address Register (MADR) \$120141**

ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	
------	------	------	------	------	------	------	--

This register contains the slave address to be used by the I<sup>2</sup>C bus (M-Bus) module. Following a reset this register is set to 0. Bit 0 is not defined. Full details can be found on page 7-6 of the 68307 user manual.

ADR7 - 1 address of 68307 when accessed as a slave

**I<sup>2</sup>C bus (M-Bus) Frequency Divider (MFDR) \$120143**

			MBC4	MBC3	MBC2	MBC1	MBC0
--	--	--	------	------	------	------	------

This register contains the pre-scale value used to scale the system clock to generate the I<sup>2</sup>C bus (M-Bus) clock. With a 14.7456 MHz system clock the I<sup>2</sup>C bus (M-Bus) clock frequency can be between 3390 Hz and 670 kHz. Full details can be found on page 7-6 of the 68307 user manual.

**I<sup>2</sup>C bus (M-Bus) Control Register (MBCR)****\$120145**

MEN	MIEN	MSTA	MTX	TXAK	RTSA		
-----	------	------	-----	------	------	--	--

This register can be read or written at any time. For a full description of this register please see page 7-7 of the 68307 user manual.

MEN	enable the I <sup>2</sup> C bus (M-Bus) module
MIEN	if set then I <sup>2</sup> C bus (M-Bus) interrupts are enabled.
MSTA	selects the mode of operation of the I <sup>2</sup> C bus (M-Bus) module.
MTX	selects the direction of transfer for master and slave transfers.
TXAK	determines whether an acknowledge signal is placed in the 9th clock bit of the data for both master and slave receivers.
RSTA	if this bit is set then a repeated start condition is placed on the bus while the MC68307 is the master.

**I<sup>2</sup>C bus (M-Bus) Status Register (MBSR)****\$120147**

MCF	MAAS	MBB	MAL		SRW	MIF	RXAK
-----	------	-----	-----	--	-----	-----	------

This is a read only register except the MIF and MAL bits which can be cleared by writing to them. At reset this register reads 0. Full details can be found on page 7-9 of the 68307 user manual.

MCF	cleared while data is being transferred. It is set on the 9th clock of a byte transfer.
MAAS	set if the 68307 is being addressed as a slave
MBB	set when the I <sup>2</sup> C bus (M-Bus) is busy.
MAL	set when arbitration is lost.
SRW	indicates the value of the R/W command bit of the calling address sent from the master.
MIF	set when there is an interrupt pending.
RXAK	cleared if an acknowledge has been received.

**I<sup>2</sup>C bus (M-Bus) Data I/O Register (MBDR)****\$120149**

This register contains data that is to be either placed on the bus or has just been read from the bus. Details can be found on page 7-10 of the 68307 user manual.



## 7.2 Eprom Size LK1, LK2, LK3, LK10,LK11

These three way links are used to configure the type of EPROM fitted to the 307-Module. Both EPROMs must be the same size. The link settings are the same for Flash EPROMs of the same size. The table below shows the link settings that are required for each EPROM size that can be fitted on the 307-Module.

Eprom Size	Eprom Type	LK11	LK10	LK1	LK2	LK3
32 k-byte	27C128	North	South	South	North	East
64 k-byte	27C256	North	South	South	North	West
128 k-byte	27C512	North	South	South	South	West
256 k-byte	27C010	North	South	North	South	West
512 k-byte	27C020	North	South	North	South	West
1 M-byte	27C040	North	North	North	South	West
2 M-byte	27C080	South	North	North	South	West

## 7.3 Watch dog Enable LK5

This two way pin header enables the watch dog. If this link is fitted then the watch dog must be toggled periodically to prevent the 307-Module being reset.

## 7.4 External Reset LK6

This two way pin header enables the 307-Module to be reset by an external source such as a reset button. It is connected in parallel to the reset (RST) in the 50 way I/O bus connector.

### **7.5 Battery Backup Enable LK7**

This two way link should be fitted at all times when the 307-Module is powered up. When the power is turned off this link can be removed to allow the battery backed RAM to clear. This should be done if the RAM becomes corrupted and the Module will not start up. In order to clear the RAM the power and this link must be removed for about 1 minute as the decoupling capacitors on the RAMs can store enough charge to power the RAMs for some time.

### **7.6 Serial Port Selection LK8, LK9**

These two links determine whether the 307-Module receives characters from the RS-232 or RS-485 serial port connector. Data is transmitted from both connectors. LK8 determines the source of the RxD signal and LK9 determines the source of the CTS signal. When both links are North then RS-232 receiver is enabled, when South the RS-485 receivers are used.

### **7.7 Ground Reference TP1**

This test point can be used as a ground pin for connecting up test equipment.

### **7.8 Real Time Clock Calibration TP2**

This test point is used to calibrate the Real Time Clock. By adjusting the variable capacitor C2, this frequency can be adjusted. It is factory set to 1 Hz.

### **7.9 Analogue Reference Voltage TP3**

This test point is used to set the analogue reference on the 307-Module. By adjusting the potentiometer R1 this reference can be modified. It is factory set to 2.560 Volts.

### **7.10 Halt LED D1**

This red LED will come on when the CPU is halted. This can occur if the 307-Module tries to access an illegal instruction. It will also flash as the Module is reset.

### **7.11 Watch Dog Input LED D2**

This red LED will light up when the watch dog times out. This will occur when the Module is reset using the reset link or the watch dog times out and LK5 is fitted.

### **7.12 Watch dog Trigger LED D4**

This green LED is connected to the watch dog trigger output. When the watch dog is toggled this LED will flash. It will also flash during power up as the watch dog is toggled to prevent the 307-Module being reset if LK5 is fitted while it powers up.

## 8 Connectors

### 8.1 I/O Connector PL1

This connector is a 50 way vertical box header. It will mate with standard IDC connectors with a central bump.

Signal	Pin Number	Pin Number	Signal
+5 Volts	50	49	+5 Volts
+12 Volts	48	47	-12 Volts
N/C	46	45	RST
N/C	44	43	DAC
CH24	42	41	AGND
CH23	40	39	Ain3
CH22	38	37	Ain2
Ain1-	36	35	Ain1+
Ain0-	34	33	Ain0+
CH130	32	31	AGND
CH21	30	29	CH20
CH19	28	27	CH18
CH17	26	25	CH16
CH132/T2in	24	23	CH131/T1in
CH129	22	21	GND
CH15	20	19	CH14
CH13	18	17	CH12
CH11	16	15	CH10
CH9	14	13	CH8
CH128	12	11	GND
CH7	10	9	CH6
CH5	8	7	CH4

Signal	Pin Number	Pin Number	Signal
CH3	6	5	CH2
CH1	4	3	CH0
GND	2	1	GND

+5 Volts	5 Volt power supply
GND	Ground connections for power supplies
+12 Volts	Only used by external signal conditioning
-12 Volts	Only used by external signal conditioning
CH0 - CH24	I <sup>2</sup> C (M-bus) digital I/O channels
CH128 - CH132	MC68307 digital I/O channels
Ain0 - Ain3	Analogue to Digital inputs
Ain0- - Ain1-	Analogue inputs if using differential mode
DAC	Digital to Analogue converter output
AGND	Analogue Ground
RST	External reset input

## 8.2 I<sup>2</sup>C (M-bus) Connector PL2

This connector is made up of a 4 way pin strip on a 0.1" pitch.

Pin Number	Signal
1	+5 Volts
2	SDA
3	SCL
4	GND

SDA	I <sup>2</sup> C (M-bus) Data line
SCL	I <sup>2</sup> C (M-bus) Clock Line

### 8.3 Keypad Connector PL3

This connector is made up with a 16 way pin strip. These sixteen digital I/O lines can be configured to scan a matrix keypad. Some of the digital channels on this connector are also on the 50 way I/O bus connector. Such channels are connected together on the 307-Module.

Pin Number	Signal
1	CH31
2	CH30
3	CH29
4	CH28
5	CH27
6	CH26
7	CH25
8	CH24
9	CH23
10	CH22
11	CH21
12	CH20
13	CH19
14	CH18
15	CH17
16	CH16

#### 8.4 RS-485 Serial Port Connector PI4

This connector is a 14 pin vertical box header. It will mate with the standard IDC connectors with a central bump. Only one of the two serial port connectors should be used at a time.

Signal	Pin Number	Pin Number	Signal
N/C	14	13	GND
N/C	12	11	VCC
RTS-	10	9	RTS+
CTS-	8	7	CTS+
TXD-	6	5	TXD+
RXD-	4	3	RXD+
N/C	2	1	N/C

RXD-	Negative receiver input
RXD+	Positive receiver input
TXD-	Negative transmitter output
TXD+	Positive transmitter output
RTS-	Negative RTS output
RTS+	Positive RTS output
CTS-	Negative CTS input
CTS+	Positive CTS input

## 8.5 Liquid Crystal Display Connector PL5

This connector is a 16 pin vertical box header. It will mate with the standard IDC connectors with a central bump. This will allow alphanumeric LCDs to be connected directly to the 307-Module. Using an adapter graphics LCDs or vacuum fluorescent displays can be used. When using a 2 line LCD pins 15 and 16 on this connector are not used.

Signal	Pin Number	Pin Number	Signal
E2	16	15	E1
D7	14	13	D6
D5	12	11	D4
D3	10	9	D2
D1	8	7	D0
E1	6	5	R/W
RS	4	3	Vcont
+5 Volts	2	1	GND

E1	Enable for the top 2 lines
E2	Enable for the lower 2 lines
D7 - D0	Data bus (buffered)
RS	Register select (A1 buffered)
R/W	Read / Write line (buffered)
Vcont	Contrast voltage

## 8.6 Module Bus expansion PL6

This is a 90 degree 64 way DIN41612 ab connector. It will mate with a range of connectors for either backplane mounting or ribbon cable connections.

Pin Number	Row b	Row a
1	D0	D8
2	D1	D9
3	D2	D10
4	D3	D11
5	D4	D12
6	D5	D13
7	D6	D14
8	D7	D15
9	GND	GND
10	CLK	SCL
11	GND	A17
12	DS1	NRST
13	DS0	A18
14	WRITE	A19
15	A20	A0
16	DTACK	RD
17	GND	WR
18	PAS	NMI
19	MAS	I4
20	ALE	I3
21	IACK	I2
22	A16	I1
23	SDA	A15

Pin Number	Row b	Row a
24	A7	A14
25	A6	A13
26	A5	A12
27	A4	A11
28	A3	A10
29	A2	A9
30	A1	A8
31	-12 Volts	+12 Volts
32	+5 Volts	+5 Volts

D0 - D15	68000 Data bus
A1 - A23	68000 Address bus
A0	8051 Address line
CLK	Main system clock
DS0 - DS1	68000 data strobes
Write	68000 write line
DTACK	Data transfer acknowledge
PAS	Peripheral address strobe
MAS	Memory address strobe
ALE	8051 address latch enable
IACK	Interrupt acknowledge
SDA	I <sup>2</sup> C (M-bus) data line
SCL	I <sup>2</sup> C (M-bus) clock line
NRST	System reset
NMI	Non maskable interrupt
I1 - I4	Open collector interrupt inputs

### 8.7 RS-232 Serial Port Connector PL7

This is a 10 way vertical boxed header. It will mate with a standard IDC connector with a central bump. If used with a 10 way IDC connector at one end and a 9 pin D type connector at the other this serial port can be connected directly to a P.C.

Signal	Pin Number	Pin Number	Signal
N/C	10	9	GND
N/C	8	7	N/C
RTS	6	5	RXD
CTS	4	3	TXD
+5 Volts	2	1	N/C

RXD	Receiver data input
TXD	Transmitter data output
RTS	RTS handshake output
CTS	CTS handshake input

### 8.8 Power PL8

This is a four way screw terminal block. The +12 Volt and the -12 Volt signals are not required for the 307-Module but they may be needed on some external signal conditioning.

Pin Number	Signal
1	+12 Volts
2	+5 Volts
3	GND
4	-12 Volts

## **9 Specification**

### **9.1 Processor**

MC68307 CMOS 68K compatible micro-controller.  
14.7456 MHz operation.

### **9.2 Memory**

Up to 2 M-byte of EPROM in 32 pin JEDEC socket.  
Up to 2 M-byte of Flash EPROM (optional).  
Up to 512 k-byte of battery backed SRAM.

### **9.3 Serial Port**

1 RS-232 buffered serial port.  
1 RS-485/422 buffered serial port.  
75 to 38400 baud.  
Hardware handshaking.  
Auto transmitt enable.

### **9.4 Digital I/O**

37 digital I/O channels.  
4 8-bit ports on I2C (M-bus).  
1 5-bit port from 68307 controller.  
Edge detection.

I2C (M-bus) I/O.  
Interrupt of change of state.  
Input low voltage -0.5V to 1.5V @ 400 $\mu$ A.  
Input high voltage 3.4V to 5.5V @ 400 $\mu$ A.  
Output low current 25mA typ.  
Output high current 100 $\mu$ A typ.

### **9.5 Timer/Counters**

Two independent 16-bit devices.  
Two match/count/capture/event registers.  
Can be used as digital I/O lines.  
Seperate input/output pins.

### **9.6 Interrupts**

One non maskable interrupt input.  
Four user interrupts that can be used as digital I/O lines.  
Software programmable interrupt levels.

### **9.7 Real Time Calendar Clock**

0.01 second resolution.  
Seconds, minutes, hours.  
Date, weekday, month, year.  
Timer.  
Alarm.  
Interrupts.

### **9.8 Power Fail Detector**

The 307-Module will be reset when the power supply falls below 4.7 Volts.

### **9.9 Watch dog Timer**

400ms time out period MAX691 watch dog.  
software programmable period for 68307 internal watch dog (normally disabled).

### **9.10 Analogue Interface**

Four 8-bit inputs.  
One 8-bit output.  
0 - 2.55 Volt input range.  
On board reference.  
Single ended or differential operation.

### **9.11 LCD Port**

5 Volt only displays.

Alphanumeric LCDs up to 4 lines of 40 characters.  
Graphics LCDs (with an adapter) up to 128 x 256 dots.  
Vacuum fluorescent displays (with an adapter).

### **9.12 I<sup>2</sup>C (M-bus) Serial bus**

High speed synchronous serial communication to dedicated peripheral ICs.  
Compatible with digital I/O, analogue I/O, LCD, video, memory etc.

### **9.13 Module Bus expansion**

Provides all signals required to expand the 307-Module's functionality.  
Standard expansion boards include serial, memory, analogue, digital, video etc.

### **9.14 Size**

100 x 118 x 15 mm

The height (15mm) does not include any mounting or cable clearances.

### **9.15 Power Supply**

5 Volt only operation.  
150 mA @ 5 Volts running.  
+/- 12 Volts for signal conditioning only.

### **9.16 Operating Temperature**

0 to 60 deg C

## 10 Appendix

### 10.1 Useful Data Sheets

MC68307 User Manual (Motorola)

This is supplied in Acrobat format on the disk version of this manual.

MC68681 Serial Port (Motorola)

The serial port used by the 68307 is basically half of an MC68681.

PCF8574 8 bit I/O expander (Philips Components)

This data sheet is for the I<sup>2</sup>C (M-bus) 8 channel digital I/O devices.

PCF8583 Real Time Calendar Clock (Philips Components)

This data sheet is for the real time clock used on the 307-Module.

PCF8591 8-bit Analogue Acquisition device(Philips Components)

This data sheet is for the I<sup>2</sup>C (M-bus) device that is used for the conversion of analogue signals.

RS Data sheet 6569 (RS Components)

This data sheet covers the RS range of alphanumeric LCDs that can be used with the 307-Module.

## 10.2 Compatible LCDs

This section lists a number of displays that can be used with the 307-Module. There may be others that will work correctly but remember that they must be 5 Volt only displays.

### 40 character x 2 lines

Handok	HDM-40216H-2
Optrex	DCM40218
RS Components	RS 588-538
Varitronix	MDL-40266

### 40 character x 4 lines

Varitronix	MDL-40466	
Seiko Epsom	M4024	with an adapter

### Graphic LCDs

The 307-Module can be used with a range of graphics LCD panels, but an adapter board is required and the programmable device is changed (K-307G).

Hitachi	LMG638x series	256 x 64 dots
Hitachi	LMG640x series	240 x 128 dots

### Vacuum Fluorescent Displays

The 307-Module can be used with the following VFD with an adapter board. Again a different programmable device will be required (K-307V).

ISE Electronics Corp.	CU20026SCPB-S	RS Components 589-339
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