



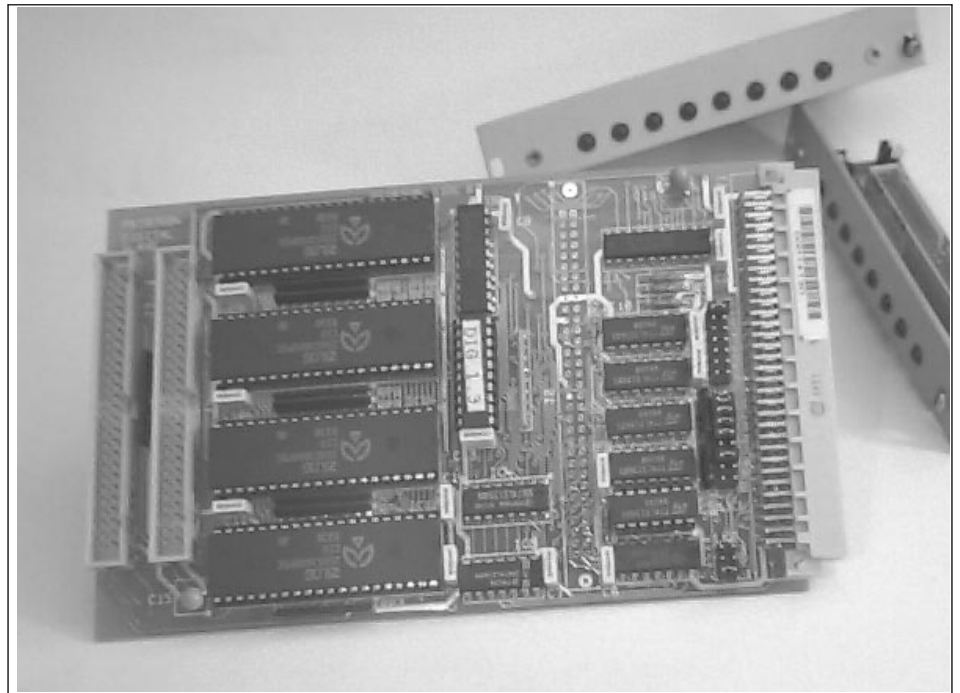
# VMEbus Digital I/O

Slave Digital Input/Output for  
VMEbus and Mini-Module Systems

The picture shows the 80 Channel Digital board with some LED monitor boards.

## Features

- ❑ Eight independent 8-bit I/O ports
- ❑ Four 4-bit special purpose I/O ports
- ❑ Polarity control
- ❑ Direction on individual bits
- ❑ Edge detection
- ❑ TTL or open-drain output
- ❑ Four handshaking modes
- ❑ IEEE-488 instrument bus 3-wire handshaking
- ❑ Request/Wait high speed transfers
- ❑ Pattern recognition logic
- ❑ Full vectored interrupts
- ❑ Twelve 16 bit counter/timers
- ❑ Pulsed, one-shot and square waves
- ❑ Count input, output, gate and trigger
- ❑ Retriggerable or no-retriggerable
- ❑ Software drivers for 68K and Mini-Module systems
- ❑ 'C' library of examples
- ❑ A16/D8, 256 byte short address space
- ❑ VMEbus Slave Rev C.1
- ❑ 3U single-height Euro-card 100\*160mm



## Description

The V-700 single height euro-card provides digital interfacing to VMEbus and Module Bus systems. The card is designed to provide enough general purpose digital I/O to satisfy most counter/timer and parallel I/O needs encountered in system design and in real-time applications. The card has 80 bi-directional TTL compatible digital signals on two industry standard 50 way IDC type connectors. This connector will accept the large range of digital signal conditioning cards available on the market.

The design is based on four Z8536 digital chips. Each of these features programmable polarity, direction, pulse catchers, open drains, handshake modes and pattern recognition. They can be used as simple TTL level I/O lines or, for example, programmed to perform the 3-wire handshaking of the IEEE-488 instrumentation bus. Each bit can be active high or low and be an input or an output.

To help with event timing or wave form generation there are also twelve 16-bit timers each with count input, output, gate and trigger control lines. A constant register is used to hold the initial timer value and a counter register for the actual counting. Retriggerable or non-retriggerable pulsed, one-shot and square wave cycles can be programmed. Four port pins are used as external access lines for each counter/timer.

The card has 12 programmable interrupt vectors. The 4 Z8536's have daisy chain priorities each containing 3 vectors corresponding (highest to lowest) to a timer, port A or port B interrupt. The vectors can optionally further define the actual source. (e.g.. timer 1,2 or 3).

The digital signals use two industry-standard I/O buses. These buses connect via a 50 way IDC cable to a large range of digital signal conditioning cards. (e.g.. opto-coupled I/O, relays, AC/DC control).

The drawing opposite is a block diagram of the Digital I/O board.

## Specification

### Digital I/O channels

80 bits in two groups

8 8-bit ports

4 4-bit ports

### Programmable

polarity

direction

1's latching inputs

open drain outputs

8-bit ports

pattern recognition

polarity

transition

mask

handshaking

3-wire IEEE-488 bus

double/single buffered

pattern match

interlocked

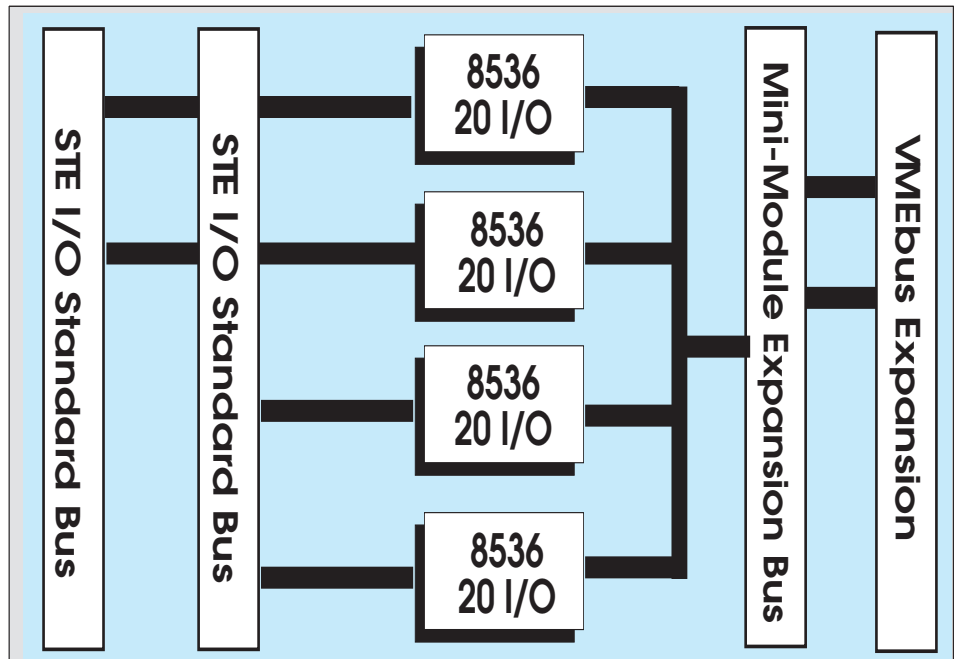
strobed

pulsed

### Counter/Timers

12 16-bit registers

continuous/single cycle



external

output  
count  
trigger  
gate

### Address decoding

256 bytes short address space

### Connectors

2 50-way I/O bus IDC connector

96-way VMEbus connector

### Power Requirements

+ 5 Volts 1200mA (typ)

### Temperature Range

0 to 70 degC

### Humidity

0 to 90%RH (non condensing)

### Size

3U Euro-card 100\*160mm

retrigger/non-retrigger

duty cycles

### VMEbus Slave Interface

Rev.C.1

Data transfer

A16:D08

Modifiers

\$29,\$2D

Interrupter

IRQ(k) k=1,..7

## Order codes

### Module Version

K-700 Module Bus 80 Channel Digital I/O card

### VMEbus Version

V-700 VMEbus 80 Channel Digital I/O card

### Miscellaneous

MV-700 Technical Manual

DAZ8036C10 Technical Manual Z8036 CIO

V700 970307



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