



# 68000/68010 CPU

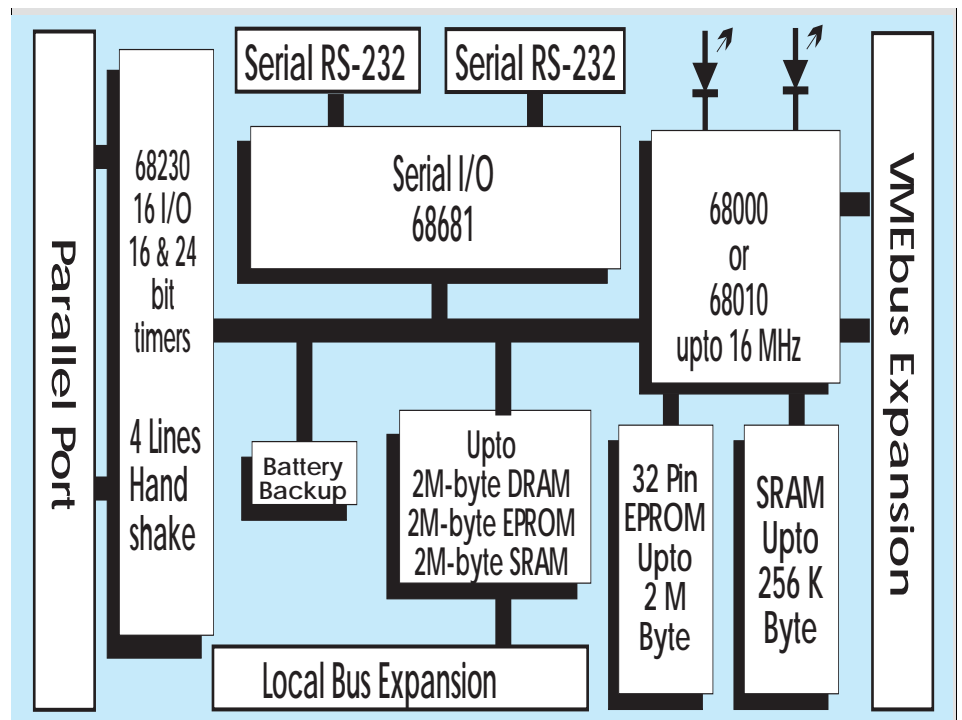
Master CPU and System Controller  
for VMEbus systems

## Features

- 68010 CPU running at 10MHz
- 68000 CPU running at 8/10MHz
- Two 32 pin EPROM sockets up to 2 M Byte
- Two 32 pin RAM sites up to 256K Byte battery backed CMOS RAM
- Debug Monitor and loader option SFT-V100
- OS-9 68K support on CMS VMEbus 68000 systems
- VMEbus Master and Controller Rev C.1
- High performance, multi-user, development system CPU
- Two RS-422/423 serial ports
- 16-bit parallel I/O port compatible with digital signal conditioning cards
- 24-bit and 16-bit hardware timers
- Real Time Calendar Clock (battery backed)

### Local expansion bus options

- 2MB DRAM (no wait states),
- 512KB DRAM (no wait states)
- 68881 co-processor
- 1MB SRAM



## Description

The V-100/10 System Processor is a single height VMEbus Master CPU and system controller running at 8/10MHz. This card has specifically been designed as a high functionality target card for automation and control systems. It contains enough EPROM and RAM to run large compiled programs (eg 'C'), in stand alone turnkey situations. It will also act as a system Master and controller in a larger system with one or more processor boards. The card is available on its own, with optional debug monitor and down loader or with the OS9 operating system.

The card can be developed on its own using a machine code debugger and down loader (SFT-V100) or in the OS9 development system (V-3000). The debugger uses one of the serial ports to connect to a host computer. The object code produced from the host is down loaded to the target CPU for testing.

Developing under OS9 allows the CPU to run multi-tasking high level languages and produce stand alone code.

Two serial ports provide RS422/RS423 communication from 50 to 38.4KBaud. Two 9-bit parallel ports, are pin compatible with the standard I/O bus connector and can be connected to the digital signal conditioning cards. Two hardware timers provide timed interrupts, pulse counter inputs etc. The real time clock provides a date and time-of-day reference for the operating system and/or application programs.

The local expansion bus options include a 1M Byte static RAM card, 512K and 2K Byte DRAM card and a 68881 floating point chip. The memory has zero wait states. This important systems feature means programs will run independently of the back plane and hence will run significantly faster.



## Specification

### Processor

68000 @ 8/10 MHz

68010 @ 10 Mhz

### Memory

zero wait state

Two 32 pin EPROMs (up to 2MB)

Two 32 pin RAMs (up to 256 KB)

### Serial Ports

Two RS-422/423

### Digital I/O

Two 8-bit parallel ports

### Timers/Counters

16 and 24-bit timers

### Real Time Calendar Clock

Year, date and time-of-day

### Battery back-up

Calendar clock and SRAM

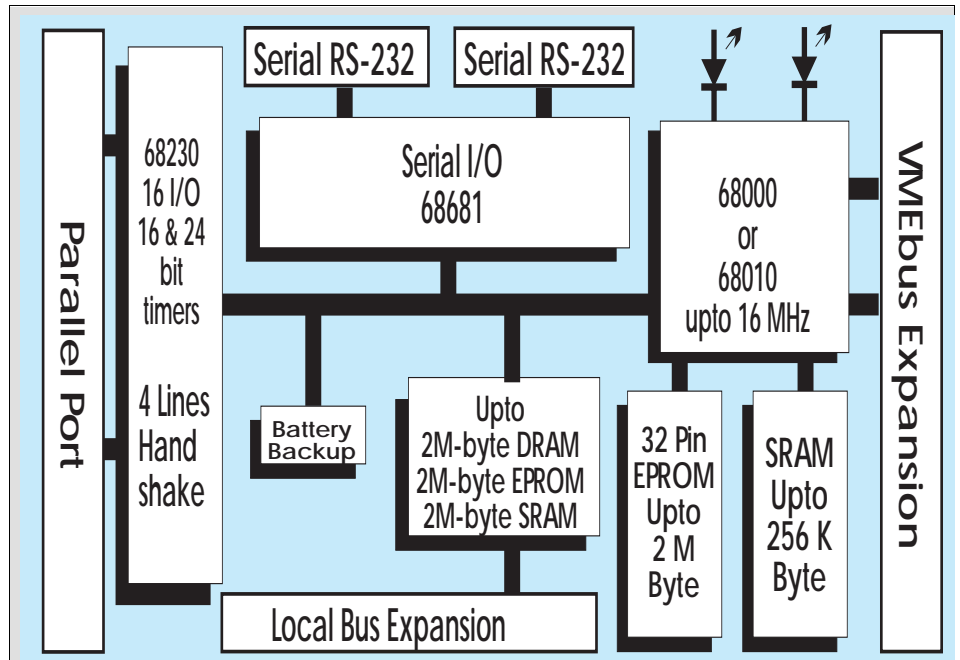
### VMEbus Master (Rev. C.1)

A24:D16 address/data

IH(1-7) interrupts

ROR (0-3) requester

Modifiers



### VMEbus Controller

SGL

BTO (32)

SYSClk

SYSRST

### Status Leds

Power on (green), Halt (red)

### Power Requirements (typ)

5V @ 1.5A, -12V @ 50mA

### Temperature/Humidity

0 to 55 C, 0 to 90% RH (nc)

### Size

3U (Eurocard 100\*160mm)

### Expansion

Zero wait states

512K or 2M Byte dynamic RAM

68881 floating point chip

1M Byte static RAM

### Optional Software

OS-9

Editor

Assembler

'C'

Modula-2

Debug Monitor

## Order Codes

V-100	68000 CPU 8 MHz 64K SRAM
VC-100	68000 CPU 10 MHz 256K SRAM
VC-110	68010 CPU 10 MHz 64K SRAM
VH-110	68010 CPU 10MHz 256K SRAM
M-102	2 MB Dynamic RAM Memory Extension
M-101	512kB Dynamic RAM Memory Extension
M-102/C	M102+68881 Co-processor
M-101/C	M101+68881 Co-Processor
M-200	1 MB Static RAM Memory Extension
SFT-V100	Debug Monitor and down loader
V-3000	OS9 Development System
MV-100	Technical Manual

V100 940308



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